

PRANEETH ACHARYA VANGALA

Ph.D. Student, Electrical Engineering

pvangala@unr.edu | www.pvangala.com | linkedin.com/in/praneeth-vangala | University of Nevada, Reno | Reno, NV, USA

PROFESSIONAL SUMMARY

Doctoral researcher in Electrical Engineering specializing in neural network architectures for power electronic converter control implemented on FPGAs. Experienced in hardware-efficient arithmetic, FPGA-MCU interfaces, and embedded control, with publications in IEEE Access, IEEE Transactions on Sustainable Computing, and MDPI Electronics. Brings university teaching experience in digital design, microprocessor, circuits, and power electronics labs, plus NSF REU graduate mentorship.

RESEARCH EXPERIENCE

Graduate Research Assistant

2025 – Present

University of Nevada, Reno | Reno, NV, USA

- Conducting doctoral research on neural network-based control architectures for power electronic converters implemented on FPGAs.
- Designed and validated a 32-bit full-duplex SPI interface between a TI TMS320F28335 MCU and an Altera Cyclone V FPGA with a handshake-based CDC architecture, achieving error-free transfer at 9.375 MHz (7.64 Mbps throughput) and $\approx 21.9 \mu\text{s}$ deterministic end-to-end latency with an RNN inverter controller.
- Designed, synthesized, and validated a resource- and power-efficient segmented Chebyshev tanh activation function in single-precision floating-point arithmetic on an Altera Cyclone V FPGA.
- Supported the PI with literature reviews, data collection, and preparation of proposals and journal/conference papers.

Graduate Research Assistant

Feb 2023 – Aug 2023

Texas A&M University-Kingsville | Kingsville, TX, USA

- Conducted research on FPGA-based hardware for recurrent neural network (RNN) controllers for power electronic converters.
- Designed, simulated, and tested a floating-point integral block in VHDL for a neural network-based power converter controller.
- Optimized a hyperbolic tangent activation function for resource usage and latency on an Intel Altera DE1-SoC FPGA.
- Implemented the McBSP serial transfer protocol between a TI TMS320F28335 DSP and an Intel Altera DE1-SoC FPGA.

TEACHING EXPERIENCE

Graduate Teaching Assistant

2025 – Present

University of Nevada, Reno | Reno, NV, USA

- ENGR 100 – Engineering Design Skills Lab:** Mentored freshman students across multidisciplinary labs (Excel, LabVIEW, materials testing, circuit design, biomedical projects); graded lab reports and provided technical guidance.
- EE 120 – Fundamentals of Electrical Engineering:** Assisted instruction in basic circuit analysis, Multisim, MATLAB, and Arduino UNO-based projects for freshman and sophomore students.
- EE 490L – Electrical Projects Laboratory:** Supported senior-level labs on active/passive filters, Arduino-based motor control, and buck/boost converters; created lesson plans, slides, and assignments, and delivered lectures.
- Managed course administration, assignments, and grading through Canvas LMS.

Graduate Teaching Assistant

Feb 2023 – Dec 2023

Texas A&M University-Kingsville | Kingsville, TX, USA

- EEEN 4355 – Digital Systems Engineering Lab:** Led senior-level labs in VHDL-based digital design on the Intel Altera DE1-SoC FPGA, covering logic gates, multiplexers, adders, latches, flip-flops, and counters, through simulation, synthesis, and on-board testing.
- EEEN 3449 – Microprocessor Systems Lab:** Led sophomore/junior-level labs in TI MSP430 microcontroller programming using C and assembly language, supporting code development and hardware debugging; graded lab reports and assignments.

OTHER EXPERIENCE

Graduate Mentor, NSF Research Experience for Undergraduates (REU)

Summer 2025 & Summer 2026

University of Nevada, Reno | Reno, NV, USA

- Mentored undergraduate students in designing (Altium, KiCad) and fabricating (Voltera V-One PCB printer) a custom power inverter controller board.
- Guided a student in deriving the theoretical error bound of the Chebyshev tanh approximation and of the full RNN.

EDUCATION

Doctor of Philosophy (Ph.D.), Electrical Engineering

2025 – Dec 2027 (Expected)

University of Nevada, Reno | Reno, NV, USA | GPA: 3.91 / 4.0

- Research focus:** Neural network architectures for power electronic converter control on FPGAs
- Relevant coursework:** Power Electronics, Random Signals & Estimation Theory, EDA (PCB Design), Power System State Estimation

Master of Science (M.S.), Electrical Engineering

December 2023

Texas A&M University—Kingsville | Kingsville, TX, USA | GPA: 4.0 / 4.0

▪ **Relevant coursework:** Analysis of Algorithms, VLSI Circuit Design, Digital Signal Processing, Rapid Prototyping & ASIC Design, Analog IC Design, Advanced Digital Design, Power Transmission & Alternative Energy

Bachelor of Technology (B.Tech.), Electronics and Communication Engineering

September 2021

CMR Engineering College (Jawaharlal Nehru Technological University Hyderabad) | Hyderabad, India | GPA: 7.7 / 10.0

▪ **Relevant coursework:** C Programming, Operating Systems, Signals & Systems, Analog & Digital Electronics, Control Systems, Electromagnetic Theory, FPGA Programming, Switching Theory & Logic Design, Digital System Design

PUBLICATIONS

[1]

P. Vangala, X. Fu, C. Hingu, and M. Hosur, “32-bit SPI interface design between Texas Instruments MCU and Intel FPGA enabling real-time intelligent control applications,” *e-Prime – Nexus of Electrical, Electronic, and Intelligent Engineering*, Art. no. 201246, 2026, doi: 10.1016/j.eprime.2026.201246.

[2]

C. Hingu, X. Fu, P. Vangala, and S. Li, “High accuracy power aware Chebyshev-based hardware implementation of tanh function for RNN controllers,” *IEEE Trans. Sustain. Comput.*, vol. 11, no. 3, pp. 342–349, May–Jun. 2026, doi: 10.1109/TSUSC.2026.3677313.

[3]

C. Hingu, X. Fu, P. Vangala, and R. Hu, “High accuracy power optimized FPGA implementation for GELU function: A Chebyshev approach,” *Electronics*, vol. 15, no. 14, Art. no. 2981, 2026, doi: 10.3390/electronics15142981.

[4]

C. Hingu, X. Fu, P. Vangala, R. Mishan, and P. Fajri, “32-bit fixed and floating-point hardware implementation for enhanced inverter control: Leveraging FPGA in recurrent neural network applications,” *IEEE Access*, vol. 12, 2024, doi: 10.1109/ACCESS.2024.3441512.

Under Review:

[1]

P. Vangala, X. Fu, C. Hingu, and M. Hosur, “A resource- and power-efficient FPGA implementation of a segmented Chebyshev tanh activation function using single-precision floating-point arithmetic,” *Electronics*, under review, Sep. 2026.

ACADEMIC PROJECTS

Real-Time Frequency Stability Controller Using Hybrid MCU+FPGA Architecture for Microgrids

UNR Coursework

▪ Designed a deterministic five-stage VHDL pipeline on an Altera Cyclone V FPGA for signal acquisition (on-board LTC2308 12-bit ADC), DC-offset removal, FIR low-pass filtering, zero-crossing frequency estimation, and RoCoF calculation.

▪ Implemented droop-based PI supervisory control and under-frequency load shedding (UFLS) on a TI TMS320F28335 at a fixed 1 ms control period, receiving frequency estimates over a 1 MHz SPI link.

▪ Cut end-to-end latency to 9.3 ms from 17 ms (single-processor baseline); in MATLAB, improved frequency nadir from −0.571 Hz to −0.247 Hz with recovery to ±0.05 Hz in 4.95 s after a +0.20 pu step load; verified fixed-point PI, UFLS, and anti-windup via software-in-the-loop.

Graph Neural Network-Based Distribution System State Estimation

UNR Coursework

▪ Proposed a real-time DSSE framework using IEEE 1547 smart inverters as sensors for real/reactive power injections, addressing sparse measurements, low observability, unbalanced operation, and DER integration.

▪ Simulated inverter-based measurement scenarios on the IEEE 33-bus system in MATPOWER to train a GNN that estimates bus voltage magnitudes, achieving an MAE of 0.027 (IEEE 33-bus) and 0.099 (IEEE 14-bus) and benchmarked against conventional WLS estimation.

Comparative Study on Kalman Filtering for Electric Vehicle Powertrain Parameters

UNR Coursework (Team of 3)

▪ Developed a unified nonlinear state-space framework for PMSM and open-end winding induction motor with dual inverter (OEWM-DI) drives to estimate rotor speed and electromagnetic torque without mechanical sensors.

▪ Implemented EKF and UKF observers with fourth-order Runge–Kutta (RK4) discretization under a Bayesian filtering formulation, comparing their modeling requirements and estimation behavior under EV-like operating conditions.

STM32-Based Brushless DC Motor Speed Control and Analysis

UNR Coursework

▪ Controlled a BLDC motor through an electronic speed controller (ESC) using an STM32F767ZI MCU, and built a PC-based UI displaying commanded vs. actual speed with a configurable delay.

▪ Interfaced a reflective object proximity sensor to measure motor speed and characterize the pulse width–speed relationship; triggered an LED at a set propeller angle at 10% speed, then ramped speed until the LED blinking was no longer visible.

Generic Null Convention Logic (NCL) MAC Unit

TAMUK Coursework

▪ Designed and verified a generic dual-rail unsigned multiply-accumulate (MAC) unit in VHDL using the asynchronous NCL paradigm.

TECHNICAL, TEACHING, AND RESEARCH SKILLS

Languages	VHDL, Verilog, C/C++, Python, MATLAB, Java, SQL, HTML/CSS, MSP430 Assembly
Tools & EDA	Altera Quartus Prime, ModelSim, Xilinx Vivado, Code Composer Studio, STM32CubeIDE, Arduino IDE, Altium, KiCad
Simulation	MATLAB/Simulink, LTspice, PSpice, OrCAD, Multisim, LabVIEW
Embedded	MCUs: TI C2000 (F28335), TI MSP430, STM32, Arduino UNO; FPGAs: Altera Cyclone V & Agilex 5, Xilinx Artix-7
Hardware & Lab	BLDC motors, buck/boost converters, power inverters, NI ELVIS III + TI Power Electronics Board, Voltera V-One
Teaching	Lab instruction, lecture delivery, lesson planning, assignment design, grading, mentoring, Canvas LMS, MS Office
Research	Literature review, proposal/manuscript preparation, hardware verification, data collection and analysis